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Low-Voltage 0.81mW, 1-32 CMOS VGA With 5% Bandwidth Variations and −38dB DC Rejection

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ABSTRACT A CMOS low-voltage amplifier with approximately constant bandwidth and DC rejection is introduced. The design is based on the cascade of a wide linear input range OTA, an op-amp and a servo-loop with extremely large time constants. It operates with $\pm 0.45V$ supplies and a power consumption of 0.81mW in 180nm technology. The bandwidth changes only from 9.08MHz to 9.54MHz over a gain range from 1 to 32, it has a 9.8Hz low cutoff frequency and a DC attenuation of 38dBs. DC floating voltage sources are used to keep the gates of all differential pairs at a constant value close to a supply rail in order to operate the amplifier circuit with minimum supply voltage. The proposed circuit has small and large signal figures of merit $FOM_{SS} = 5380$ (MHz*pF/mW) and $FOM_{LS} = 0.0085$((V/ns)*pF/mA) for a nominal gain A = 32.

INDEX TERMS Low-voltage, low power, CMOS amplifiers, transresistance amplifier, linear transconductors.

I. INTRODUCTION

The amplifier is an essential block in analog circuits. In many applications variable gain amplifiers (VGAs) are required with DC rejection, low bandwidth variations over the gain adjustment range, reduced supply voltage and power dissipation, i. e. wireless systems [1] and biomedical systems [2].

The widely used conventional op-amp based inverting amplifier shown in Fig. 1 has a gain given by $G = -(R_2/R_1)$. The loop gain determines the bandwidth (BW) of the circuit according to the expression $BW = GB/(1 + R_2/R_1)$; where GB is the gain-bandwidth product of the op-amp. The bandwidth (BW) decreases as the gain increases (G).

A common amplifier approach that ideally has a constant bandwidth is achieved by replacing the op-amp with a current feedback operation amplifier (CFOAs) as explained in [3]. It requires CFOAs with extremely low input impedance $|Z_{in}|$ over the amplifier's bandwidth in the low impedance input terminal of the CFOA. $|Z_{in}| \ll R_1$ is very difficult to accomplish in practice. In [4] an AC-coupled ultra low-voltage

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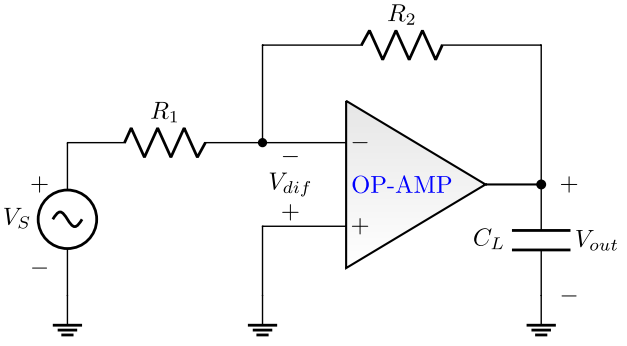

FIGURE 1. Conventional op-amp-based inverting amplifier.

VGA with constant bandwidth based on the conventional op-amp approach was presented. This configuration has DC rejection. The bandwidth is maintained constant by having a fixed negative feedback factor $\beta = 1/G_{MAX}$ independent of the selected gain G. The drawback of this approach is that it results in a constant but minimum bandwidth with value $BW = BW_{MIN} = GB/G_{MAX}$. Moreover, the AC coupling capacitors lead to frequency dependent loading of the signal

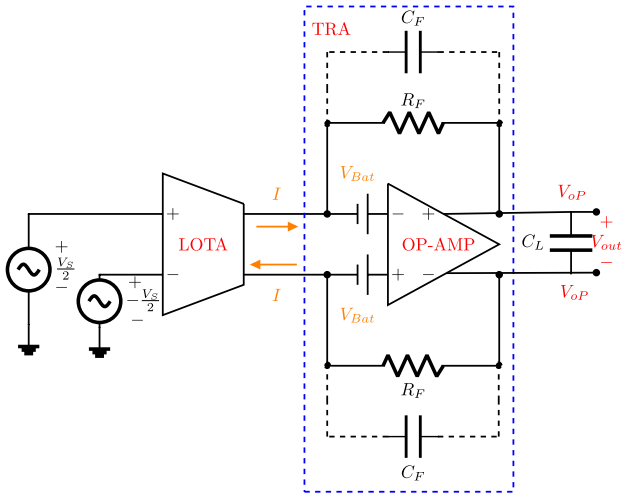

FIGURE 2. Low-voltage LOTA-TRA constant bandwidth amplifier.

source since the impedance of coupling capacitors is reduced at high frequencies.

Another alternative to achieve low bandwidth variations is the cascade combination of a linear OTA (LOTA) and an op-amp-based transresistance amplifier (TRA) as shown in Fig. 2. Using this configuration both building blocks (LOTA and TRA) as well as the combination of the two have an ideally constant and maximum bandwidth independent of the gain. We denote here this configuration as LOTA-TRA amplifier. It has been also called Cherry-Hooper amplifier [5]–[8]. The explanation of why the LOTA-TRA amplifier has low bandwidth variations over the gain adjustment range is reviewed in the following section.

In many practical situations, like in biomedical or communication systems, the signals have a very small AC component superimposed on a large DC component. In these cases the high gain required to amplify the small AC signal can also lead to amplifier saturation given that the DC components and the op-amp's offset are also amplified by the gain G. A common approach is to use AC coupled architectures to reject the DC component of the input signal, but they are difficult to implement on chip for the very low cutoff frequencies required in some applications. Servo-loops (SLs) are also used to provide the amplifier with DC attenuation [9]–[11]. The VGA with a SL circuit performs as a high-pass filter in the low frequency band attenuating all frequencies below its cutoff frequency, including the DC component of the signal and the DC offset of the op-amp. Commonly, an active SL is implemented using an integrator and the amplifier's low cutoff frequency f_L depends on the unity gain frequency of the SL integrator $f_0 = 1/(2\pi R_{Int} C_{Int})$. Where C_{Int} and R_{Int} are the capacitor and resistor used in the integrator [12], [13]. In order to have a very-low cutoff frequency (in the Hertz range) very large C_{Int} and/or R_{Int} values are needed which are very difficult to integrate on chip.

The other challenge that analog and mixed-signal circuits face is the low available supply voltage to operate ICs in modern CMOS technologies. This supply voltage has decreased as CMOS feature sizes have been scaled down; i. e. in 180nm technology the nominal supply voltage is $V_{supply} \approx V_{DD} - V_{SS} \approx 1.8$V while in 16nm technology is 0.7V. On the other hand, the threshold voltages (V_{TH}) have not decreased at the same rate. So, for the 180nm CMOS technology $V_{TH} \approx 0.55V$, while for 16nm $V_{TH} \approx 0.4$V. The headroom of the differential pair given by $HR_{DP} = V_{GS} + V_{DSsat}$, where V_{GS}, V_{DSsat} are the gate-source and drain-source saturation voltages respectively, severely constrains the input signal swing and leads to minimum supply requirements $V_{supplyMIN} = 2HR_{DP}$. The headroom of the differential pair assuming $V_{DSsat} \approx 0.1$V constraints the design to operate with a minimum supply $V_{supplyMIN} \approx 1.5$V in 180nm technology. This without considering headroom that might be required by input signal swing. In modern deep sub-micrometer CMOS technologies the situation is more adverse, so for 16nm CMOS technology this corresponds to a $HR_{DP} \approx 0.6$V and a minimum supply $V_{supplyMIN} \approx 1.2$V which is larger than the nominal supply of this technology. For this reason, conventional VGA architectures are not even functional in these technologies with transistors operating in strong inversion. Also, in higher feature size (older) CMOS technologies it is convenient to operate ICs with reduced supply voltage in order to decrease power dissipation.

In this paper we propose a low-voltage implementation of a linear VGA using a LOTA-TRA amplifier with high attenuation for DC and offset and a low cutoff frequency (f_L) in the order of Hertz. This scheme is characterized by a large differential input voltage swing and low bandwidth variations over the gain adjustment range from 1 to 32. It uses a servo-loop to attenuate the input signal DC component as well as the op-amp offset. The proposed circuit can be operated with much lower bias currents in order to be used in biomedical applications where power dissipation is the main concern. This will reduce the bandwidth as discussed in the simulation results section. However, biomedical signals require very low bandwidths. Additionally, the proposed circuit has high input impedance, therefore it does not load the signal source, so that a low impedance (buffered) signal source is not necessary as it is the case for the inverting amplifier of Fig. 1.

The paper is organized as follows: section II describes the proposed circuit. In section III simulated results in 180nm technology are discussed and conclusions are presented in section IV.

II. CIRCUIT DESCRIPTION OF THE PROPOSED VGA WITH DC ATTENUATION

A. CONSTANT BANDWIDTH OPERATION OF LOTA-TRA CIRCUIT

The proposed implementation of the low-voltage LOTA-TRA amplifier is shown in Fig. 3. It uses a wide input range low voltage linear operational transconductor amplifier (LOTA) to transform the input differential voltage V_s into complementary LOTA output currents with value $I_{OTA} = G_{m1} V_s$.

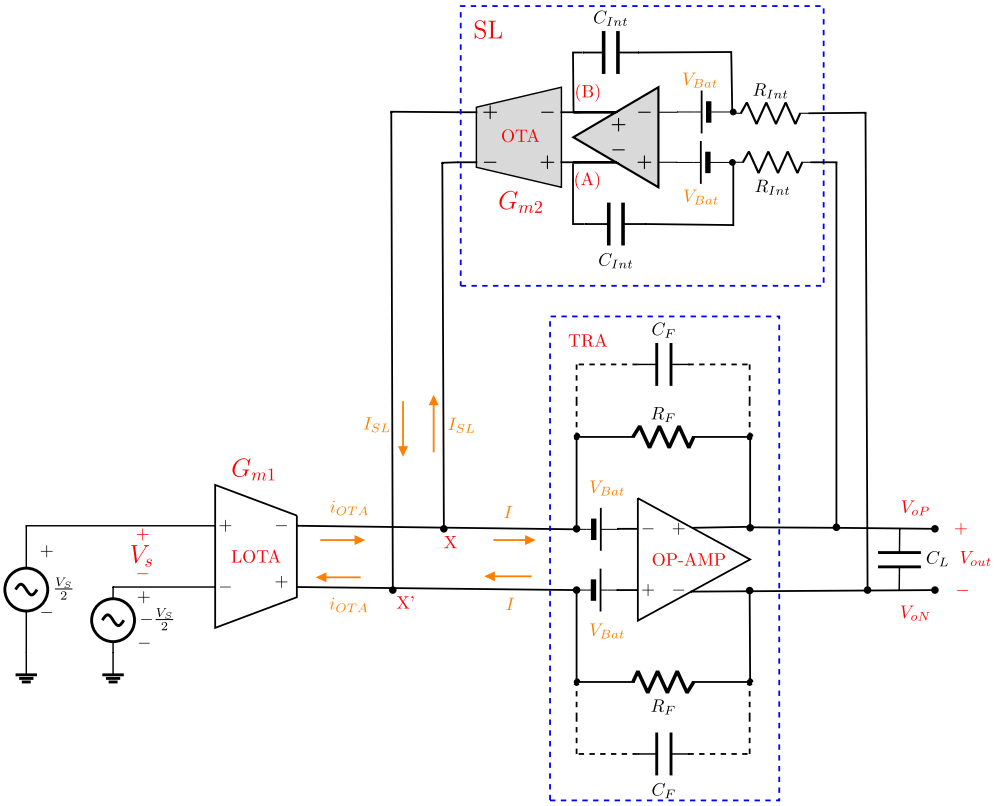

FIGURE 3. Proposed low-voltage LOTA-TRA amplifier with constant bandwidth and DC rejection.

It is important to have a linear V-I conversion, thus the OTA transconductance G_{m1} should have a linear behavior over a wide input differential range. The LOTA implementation uses two low-voltage linear current control units (LCCUs) and it is described in the following subsection. The currents generated by the low-voltage LOTA are then converted into the output voltage by an op-amp based low-voltage transresistance amplifier through feedback resistors R_F according to $V_{out} = 2I_{OTA}R_F$. The voltage gain of the LOTA-TRA amplifier is then given by $G = 2G_{m1}R_F$. The transconductance of the low-voltage LOTA is determined by a resistor R used in the low-voltage LCCU and the scaling factor N of the transistors in the output branches of the OTA as $G_{m1} = N/R$. Therefore, the low-voltage LOTA-TRA amplifier's voltage gain is given by $G = 2NR_F/R$. The TRA and LCCUs are described in detail in the following subsections.

The bandwidth of the LOTA-TRA is maintained constant because both the LOTA and the TRA have a constant bandwidth independent of the values of R_F and R that determine the VGA voltage gain. In the case of the LOTA the bandwidth is constant because the output terminals of the LOTA are connected to the low impedance input terminals of the TRA that can be seen ideally as an AC ground. Therefore, the bandwidth of the LOTA is determined only by the internal high frequency pole of the LOTA $BW_{LOTA} = f_{pOTA}$. This allows the LOTA to work with maximum and constant bandwidth. On the other hand the TRA has also a maximum and constant bandwidth independent of gain because from its point of view the LOTA performs as high impedance input current sources whose internal resistances correspond to the high output resistance of the LOTA $R_{outLOTA}$. Given that the TRA uses a Miller op-amp, the bandwidth of the TRA is given by $BW_{TRA} = GB_{op-amp}/(1+R_F/R_{outLOTA})$, for $R_F \ll R_{outLOTA}$, $BW_{TRA} \approx GB_{op-amp}$ independent of the value of R_F that determines the transresistance gain. Thus, the TRA has ideally maximum bandwidth for all values of R_F. In practice for high gain values R_F can be comparable to $R_{outLOTA}$ in which case it leads to some bandwidth reduction. This is typically avoided by connecting a capacitor C_F in parallel with R_F. This capacitor scales down as R_F increases.

The bandwidth of the LOTA-TRA amplifier $BW_{LOTA-TRA}$ is determined by the bandwidths of the LOTA and TRA and is approximated by equation (1) [14]. Since, ideally these bandwidths are constant the low-voltage LOTA-TRA also exhibits a constant bandwidth.

$$BW_{(LOTA-TRA)} = \frac{1}{\sqrt{\frac{1}{BW_{LOTA}^2} + \frac{1}{BW_{TRA}^2}}} \tag{1}$$

B. IMPLEMENTATION OF LOW-VOLTAGE LINEAR OTA

The low-voltage linear current control unit (LCCU) circuit shown in Fig. 4 is used as a core block to implement

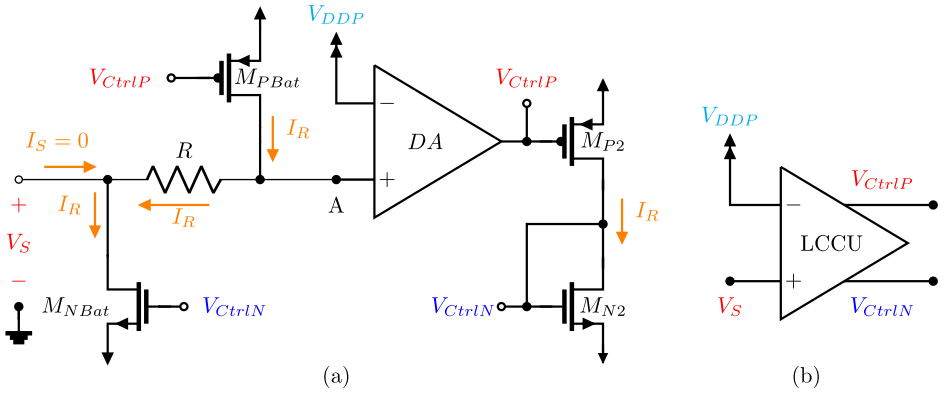

FIGURE 4. a) Low voltage linear current control unit, b) symbol.

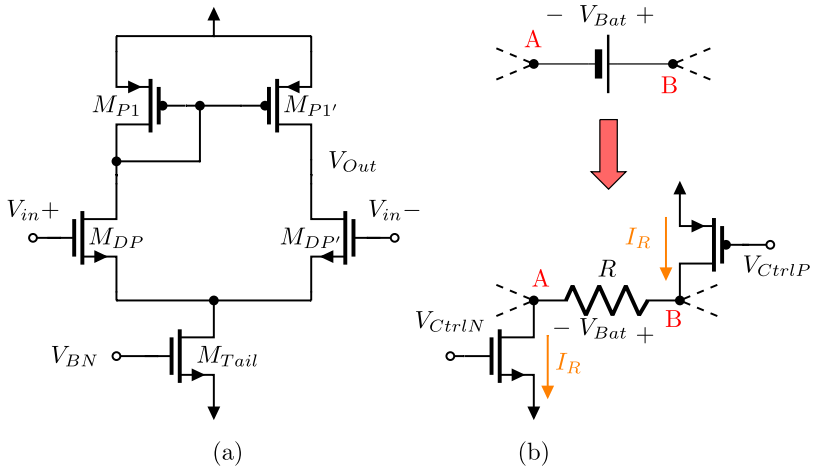

FIGURE 5. a) Differential amplifier (DA) with active load used in the V to I conversion unit, b) floating voltage source implementation.

the low-voltage LOTA and the DC floating voltage sources shown in Fig. 5b. These voltage sources allow the low voltage operation of the TRA. The LCCU circuit uses a current mirror loaded differential amplifier (DA) with NMOS input transistors, whose transistor level schematic is shown in Fig. 5a and it operates as follows:

A voltage, V_{DDP} which is very close to V_{DD}, ($V_{DDP} \approx V_{DD} - 0.07V$), is connected to the negative input terminal of the DA. Negative feedback causes the voltage V_A at the positive terminal of the *DA* to have the same value V_{DDP} at its negative input terminal. This provides a headroom for the DA with value $HR_{DP} = V_{supply} - 0.07V$ which allows the circuit to operate with very low supply voltage $V_{DD_{min}} = HR_{DP} = V_{GS} + V_{DSsat} + 0.07V$.

The output voltages of the LCCU, V_{CtrlP} and V_{CtrlN}, are connected to the gates of PMOS and NMOS transistors M_{PBat} and M_{NBat}. These transistors generate matched sourcing and sinking currents, I_R, that flow through R. I_R satisfies the conditions of eqs. (2) and (3), where $I_Q = V_{DDP}/R$ and $i_{out} = V_S/R$. The current I_R can be replicated using the voltages V_{CtrlP} and V_{CtrlN} in other branches and allows implementation of floating DC voltage sources with value $V_{Bat} = V_{DDP} - V_s$ as shown in Fig. 5b.

$$I_R = \frac{V_{DDP} - V_s}{R} = \frac{V_{DDP}}{R} - \frac{V_s}{R} \tag{2}$$

$$I_R = I_Q - i_{out} \tag{3}$$

Fig. 6 shows the implementation of a low-voltage LOTA. In this scheme two linear current control units (LCCU) whose inputs are connected to complementary input signals $V_s/2$ and $-V_s/2$ are used. They generate four control output voltages V_{CtrlP1} and V_{CtrlN1} from $V_s/2$ and V_{CtrlP2} and V_{CtrlN2} from $-V_s/2$ that drive the two output branches of the LOTA with transistor scaled by a factor N that generate offset-free complementary output currents $\pm i_{out}$ with value $i_{out} = N \cdot (V_s/R)$. In the first branch V_{CtrlP1} induces a current I_{R1} on the PMOS transistor while V_{CtrlN2} drives the NMOS transistor producing a current I_{R2} to flow on the same branch. The values of I_{R1} and I_{R2} are given by eq. (4) and (5) respectively. The difference of these two currents yields an output current $i_{out} = N \cdot (V_s/R)$. Similarly, the second branch generates a complementary output current signal $-i_{out}$. In this branch the

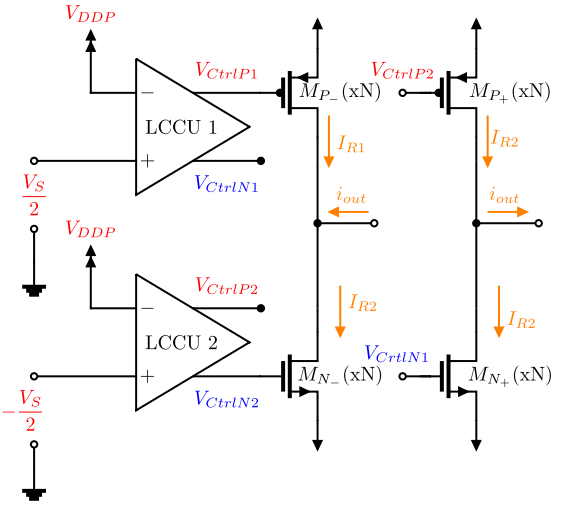

FIGURE 6. Low voltage linear OTA with complementary outputs based on two LCCUs.

LCCU1 output voltage V_{CtrlN1} drives the NMOS transistor while the LCCU2 output voltage V_{CtrlP2} drives the PMOS transistor. In practice the LOTA does not require complementary input signals $V_s/2, -V_s/2$. It also generates complementary output currents $\pm i_{out}$ with unbalanced signals V_{s1} and V_{s2} that have non-zero common mode component and whose difference is given by $V_s = V_{s1} - V_{s2}$. The common mode component is cancelled when the currents I_{R1} and I_{R2} are subtracted at the output branch.

$$I_{R1} = N\left(\frac{V_{DDP}}{R} - \frac{V_s}{2R}\right) = N\left(I_Q - \frac{i_{out}}{2}\right) \quad (4)$$

$$I_{R2} = N\left(\frac{V_{DDP}}{R} + \frac{V_s}{2R}\right) = N\left(I_Q + \frac{i_{out}}{2}\right) \quad (5)$$

C. LOW-VOLTAGE TRANSRESISTANCE AMPLIFIER

The low voltage transresistance amplifier is implemented using the two-stage fully differential free class AB Miller op-amp reported in [15] and shown in Fig. 7. Class AB operation is achieved using capacitors C_{bat} and large resistor values R_{large}. This way high speed changes are transferred from nodes V_{o1p} and V_{o1n} to nodes X and X' through capacitors C_{bat}, forcing both output transistors to be active as amplifiers and perform as a push-pull class AB amplifier with a high symmetrical slew rate at the output. In this structure the maximum positive and negative output currents are not limited by the bias currents.

To achieve low-voltage operation the input terminals V_{iP} and V_{iN} of the op-amp are DC level shifted close to a value V_{DDP}. To do so, floating voltage sources with constant value $V_{Bat} = V_{DDP}$ are used as shown in Fig.3. They are implemented using a resistor R_{Bat}, and sinking and sourcing current sources with value $I_{Bat} = V_{DDP}/R_{Bat}$ as shown in Fig. 5b. The control voltages for I_{Bat} are generated using an additional LCCU with a resistance R_{Bat} and whose input terminal is connected to ground.

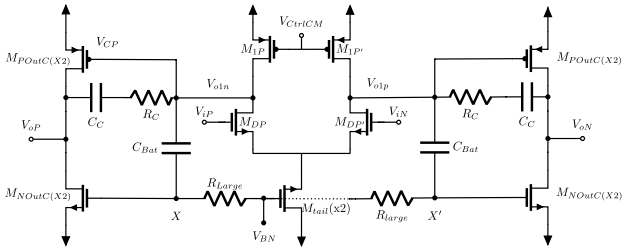

FIGURE 7. Free class AB two stage Miller op-amp.

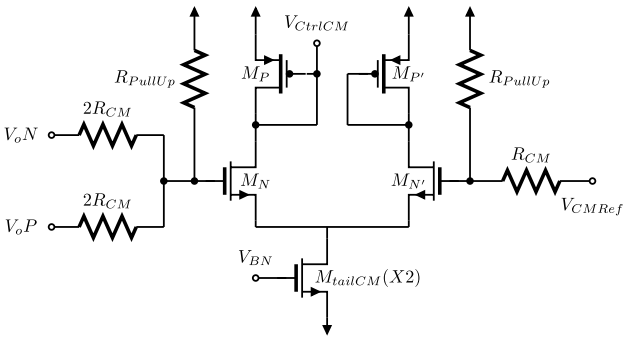

FIGURE 8. Low-voltage common mode feedback network.

A low-voltage common mode feedback network (LVCMFN) that sets the output common mode voltage of the op-amp to the midsupply voltage $V_{CMRef} = (V_{DD} + V_{SS})/2$ is shown in Fig. 8. Just as for the op-amp low voltage operation of the CMFN requires the gates of transistors M_N and $M_{N'}$ to operate at a voltage close to the upper rail. This is achieved through a resistive voltage divider formed by R_{CM} and R_{PullUp}, where pull-up resistors $R_{PullUp} \approx 0.6\, R_{CM}$ are used.

D. LOW-VOLTAGE SERVOLOOP WITH VERY LOW 3dB FREQUENCY

A servo-loop (SL) is used to obtain a high-pass characteristic in the amplifier's low frequency range that attenuates the DC component of the input signal by a large factor but that amplifies signals starting at very low frequencies. The block diagram of the circuit including the servo-loop that uses an integrator and a transconductor is shown in Fig. 9. This configuration yields to the system transfer function described by equation (6), where H_{TRA} and H_{Int} are the transfer functions of the TRA and the integrator respectively. The transfer function of the TRA is defined by equation (7), where ω_{3TRA} is its 3dB frequency and the transresistance gain is defined by the feedback resistor R_F. The transfer function of the integrator is given by (8). In practice the integrator as a low-pass response with DC gain A_{OLInt} and a 3dB frequency $\omega_{3Int} = \omega_0/A_{OLInt}$, where ω_0 is the unity gain frequency of the integrator given by $\omega_0 = 1/R_{Int}C_{Int}$.

The frequency response of the proposed LOTA-TRA circuit with servoloop is depicted in solid line in Fig. 10 and defined by equation (9), where G_{m1} and G_{m2} are the

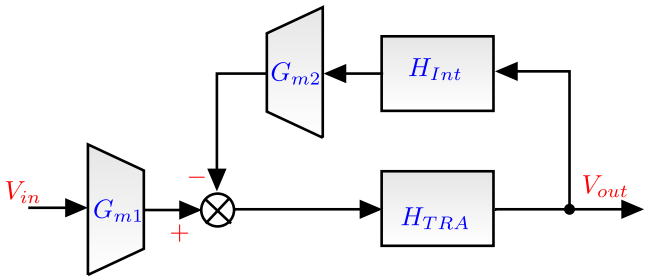

FIGURE 9. Block diagram of the servoloop.

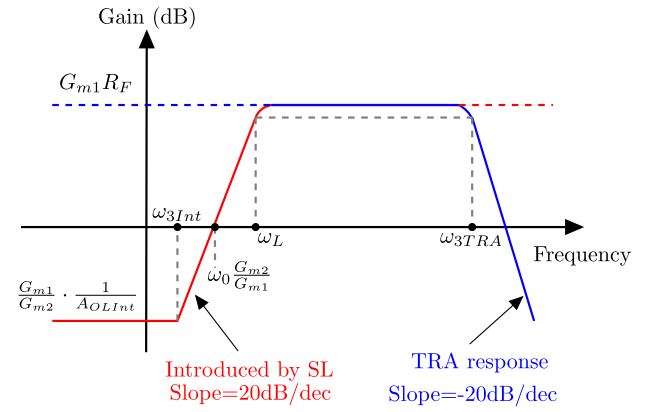

FIGURE 10. Frequency response of the proposed LOTA-TRA circuit with servoloop.

transconductance gains of the input LOTA and the feedback transconductor respectively. It is assumed that $\omega_{3Int} \ll \omega_L \ll \omega_{3TRA}$, where ω_L is the low cutoff frequency of the VGA. The response of the integrator is inverted due to the fact that it is used in the negative feedback path of the amplifier. The low-pass response of the integrator provides the amplifier with the high-pass characteristic at low frequencies. For DC ($\omega = 0$) the SL has a gain $A_{OLInt}G_{m2}$ leading to a high DC attenuation with value $H^*(0) = G_{m1}/(G_{m2}A_{OLInt})$ as expressed by equation (10). It has a zero and a pole in the low frequency range at ω_{3Int} and ω_L respectively, where $\omega_L = \omega_0 G_{m2}R_F$ (11). The amplifier has a unity gain in the low frequency band at $(G_{m2}/G_{m1})\omega_0$ as described by equation (12). At $\omega = \omega_L$ the SL begins to have a negligible effect over the response of the amplifier, the gain is given by equation (13). At $\omega \gg \omega_L$, the servo-loop has very low gain and the transfer function of the VGA at these frequencies can be approximated by equation (14). It can be seen that ω_{3TRA} is the 3dB frequency in the high frequency range. In order to achieve very low frequencies ω_L (in the hertz range) the servoloop requires the unity gain frequency of the integrator ω_0 to be much smaller than ω_L, $\omega_0 \ll \omega_L$. Very low values for ω_0 (in the sub-hertz range) can be obtained on chip by implementing R_{Int} with quasi-floating gate transistors [16], [17] that have equivalent resistance values R_{Int} on the order of hundreds of GΩs which in combination with typical integrated capacitor C_{Int} in the order of pF leads to the required time constants in the order of seconds. If constant values for ω_L independent of the gain are required C_{Int} can be implemented as a digitally programmable capacitor array that scales C_{Int} with R_F So that the ratio R_F/C_{Int} that determines ω_L remains constant with changes in R_F.

$$H(j\omega) = \frac{V_{out}}{V_{in}} = \frac{G_{m1}H_{TRA}}{1 + G_{m2}H_{Int}H_{TRA}} \tag{6}$$

$$H_{TRA}(j\omega) = \frac{-R_F}{1 + \frac{j\omega}{\omega_{3TRA}}} \tag{7}$$

$$H_{Int}(j\omega) = \frac{A_{OLInt}}{1 + \frac{j\omega}{\omega_{3Int}}} \tag{8}$$

$$H(j\omega) = \frac{G_{m1}}{G_{m2}A_{OLInt}} \cdot \frac{\left(1 + \frac{j\omega}{\omega_{3Int}}\right)}{\left(1 + \frac{j\omega}{\omega_L}\right)\left(1 + \frac{j\omega}{\omega_{3TRA}}\right)} \tag{9}$$

where

$$|H(0)| = \frac{G_{m1}}{G_{m2}} \cdot \frac{1}{A_{OLInt}} \tag{10}$$

$$|H(\omega_{3Int})| = \frac{G_{m1}}{G_{m2}} \cdot \frac{\sqrt{2}}{A_{OLInt}} \tag{11}$$

$$\left|H\left(\frac{G_{m2}}{G_{m1}}\omega_0\right)\right| = 1 \tag{12}$$

$$|H(\omega_L)| = \frac{G_{m1}R_F}{\sqrt{2}} \tag{13}$$

$$H(j\omega) \approx G_{m1}H_{TRA} \approx \frac{G_{m1}R_F}{1 + \frac{j\omega}{\omega_{3TRA}}} \tag{14}$$

The transistor level schematic of the low voltage integrator is shown in Fig. 11. It uses resistors $R_{LCMF} = 100k\Omega$ as a local common mode feedback (LCMF) [18] and has a DC gain $A_{Int} = g_{m1}(R_{LCMF}||r_{o1}||r_{o3})$. Similar to the op-amp in the TRA, low voltage operation is achieved by inserting floating DC batteries with values V_{DDP} in series with transistors M1 and M1'. This DC shifts their gates close to the upper rail.

The schematic of the SL transconductor is shown in Fig. 12. It consist of a differential amplifier with active loads and a transconductance gain G_{m2}. In order for this circuit to operate with low supply voltage it is required that the DC operating of nodes A, B at its inputs are close to V_{DD}. This is achieved by inserting a diode connected transistor M_{Shift} with very small bias current in the integrator. This transistor acts as a floating battery with approximate value of V_T that DC shifts the output nodes (A) and (B) of the integrator to a value close to V_{DD}.

The outputs of the integrator are connected to the inputs of the SL OTA shown in Fig 12. The SL transconductor transform the output voltage of the integrator into complementary currents I_{SL} that are subtracted at nodes X and X' from the currents I_{OTA} generated by the LOTA circuit.

III. SIMULATION RESULTS

The proposed LOTA-TRA amplifier circuit of Fig. 3 was designed and simulated using Cadence Framework II with a commercial 180nm technology CMOS n-well process design kit provided by MOSIS. This process has nominal supply voltage $V_{DDNominal} = 1.8V$ as well as PMOS and NMOS

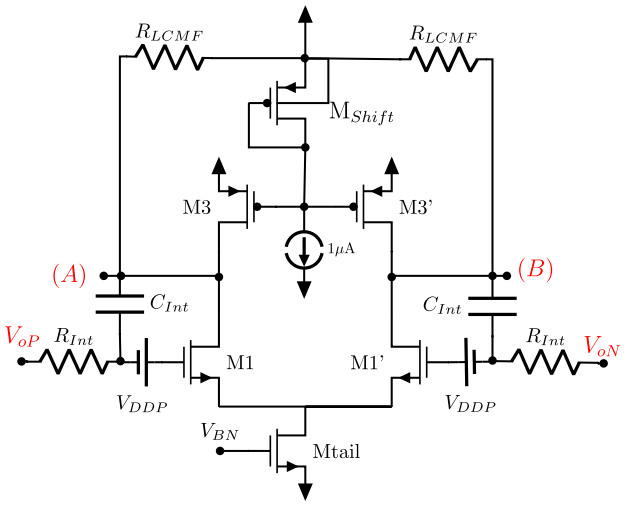

FIGURE 11. Transistor level schematic of low-voltage SL integrator with resistive local common mode feedback and output DC level shift.

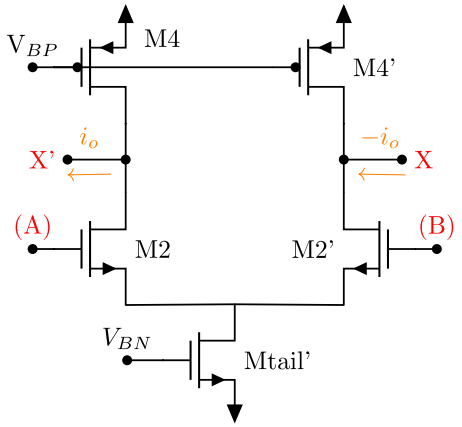

FIGURE 12. Transistor level schematic of SL OTA.

threshold voltages $V_{THn} \approx |V_{THp}| \approx 0.55V$. The designed circuit is capable to work with supply voltages as low as $\pm 0.45V$ with a total power consumption of 0.81mW and wide linear input range. The bandwidth is maintained within small variations of less than 10% across gains 1 to 32 with a DC attenuation of −38dB and constant $f_L = 9.8$Hz.

The LOTA was designed using two LCCU circuits as shown in Fig. 6 and utilizes bias currents $I_{biasLCCU} = 12.5\mu$A. The output transistors were sized with $N = 4$. The floating voltage sources V_{Bat} in the TRA and the integrator required an additional LCCU with its input connected to ground. All LCCUs use a resistor with value $R_{Bat} = 23.2k\Omega$. The fully differential op-amp of Figs. 7 and 8 was used in the TRA with bias currents $I_{Bias} = 50\mu$A. The resistances used in the CMFN of Fig. 8 have a value of $R_{CM} = 800k\Omega$. With the bias currents used, PMOS and NMOS transistors have gate-source voltages $|V_{GS}| \approx 490mV$ and $V_{DSsat} \approx 70mV$. The characterization parameters of the implemented low-voltage op-amp and LOTA circuits are summarized in Table 1 and Table 2 respectively. The integrator used in the SL has a 3dB frequency of $f_{3Int} = 11.29$mHz, a unity gain frequency $f_0 = 5.8$Hz and a DC gain $A_{OLInt} = 54.2$dB.

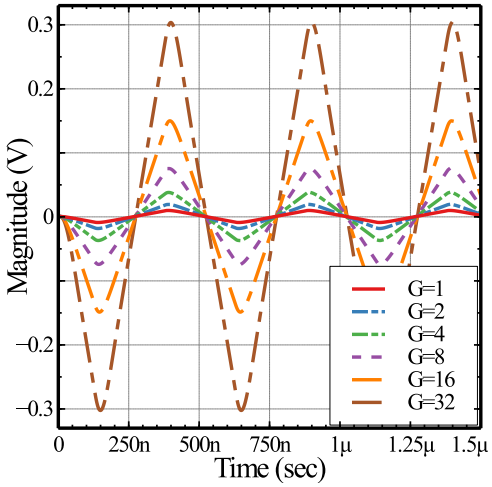

FIGURE 13. Transient simulation of proposed LOTA-TRA with SL for gains 1-32, with a triangular input that has a 50mV DC component.

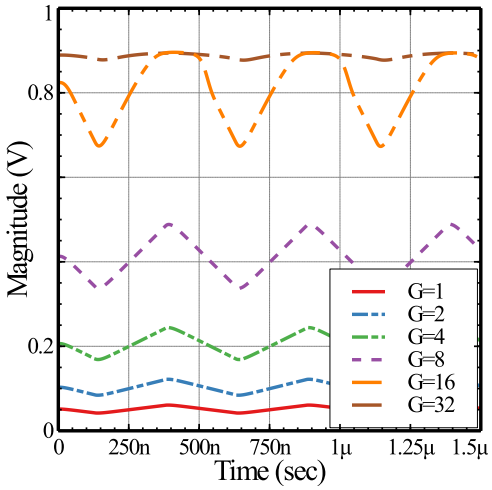

FIGURE 14. Transient simulation of proposed LOTA-TRA without SL for gains 1-32, with a triangular input that has a 50mV DC component.

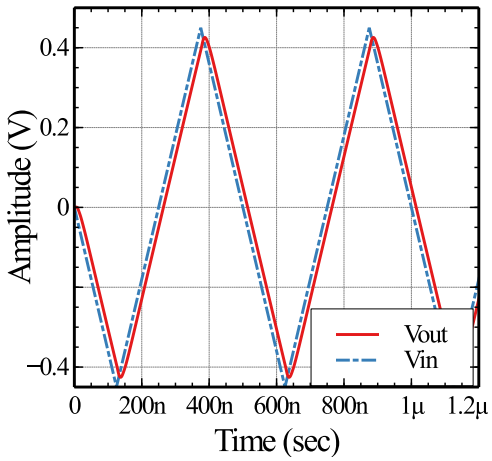

FIGURE 15. Transient analysis with 900mVpp 2MHz triangular input.

Figs. 13 and 14 show the simulated transient output voltage of the proposed low-voltage LOTA-TRA amplifier with and

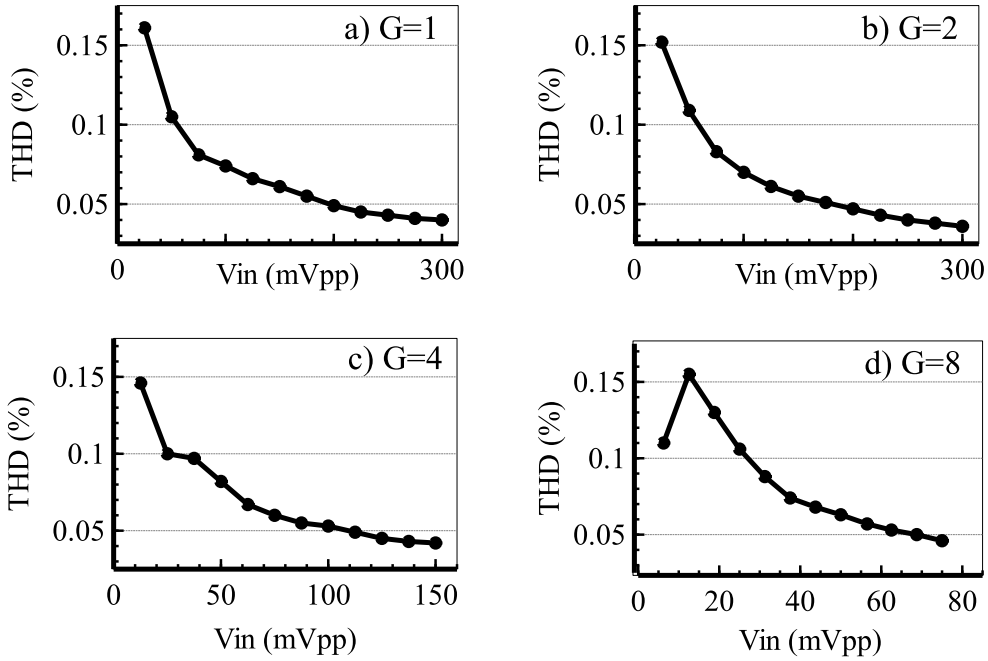

FIGURE 16. THD versus Vin simulations for different gains: a) G = 1, b) G = 2, c) G = 4 and d) G = 8.

TABLE 1. Low-voltage op-amp characteristics.

Parameter	Value	Parameter	Value
$g_{m_{DP}}$ ($\mu A/V$)	935	R_c (kΩ)	2.5
I_{total} (μA)	400	C_c (pF)	2
Supply Voltage (V)	±0.45	C_L (pF)	10
L (nm)	500	F_{3dB} (kHz)	23.72
W_P (μm)	150	GBW (MHz)	50
W_N (μm)	80	PM (°)	54.5

TABLE 2. Low-voltage LOTA characteristics.

Parameter	Value	Parameter	Value
$g_{m_{OTA}}$ (μA/V)	172	$R_{Out_{OTA}}$ ($k\Omega$)	62.5
I_{Total} (μA)	200	Supply Voltage (V)	±0.45
$L_{PMOS/NMOS}$ (nm)	500	C_L (pF)	0.5
W_P (μm)	150	A_{OL} (dB)	37.4
W_N (μm)	80	f_{3dB} OTA(MHz)	150

TABLE 3. Values of resistor R_F and capacitor C_F used in the transresitance amplifier.

VGA gain	R_F(kΩ)	C_F(pF)
1	2.9	7
2	5.8	3.7
4	11.6	1.87
8	23.2	0.98
16	46.4	0.45
32	92.8	0.1

without servo-loop, respectively. The amplifier was configured for gains ($G \approx 1, 2, 4, 8, 16, 32$) with a 20m$V_{pp}$, 2MHz triangular input signal that had superimposed a 50mV DC voltage. The gain is controlled by the value of R_F. It can be seen that the proposed circuit using the servo-loop is capable of attenuating the offset. In the version that does not have a servo-loop the offset is also amplified leading to output DC shift and saturation for high gains.

The circuit exhibits a linear behavior that is preserved for small and large input signal amplitudes as well. This is depicted in Fig. 15 where the circuit has a unity gain and a $\pm 450mV$, 2MHz triangular signal is applied at the input, linearity is maintained approximately over a range of $\pm 425mV$. The architecture has a THD = 0.047% and SNR = 66dBs with a 200mV_{pp}, 2MHz sinusoidal input signal that had a DC component of 10mV and a gain $G = 2$. Fig. 16 depicts the THD as function of the amplitude of the input signal for four different gains: a) $G = 1$, b) $G = 2$, c) $G = 4$ and d) $G = 8$.

The AC response of the proposed LOTA-TRA with SL circuit is shown in Fig. 17. The gain is varied by changing the value of R_F from 2.9kΩ to 92.8kΩ. The capacitance C_F is changed along with R_F from 0.1pF to 7pF in order to maintain the pole at ω_{3TRA} constant. Table 3 shows the values used for R_F and C_F for the different VGA gains. The circuit exhibits a 38dB attenuation at DC. The high cutoff frequency f_{TRA} has small variations ranging from 9.08MHz to 9.54MHz while the low cutoff frequency varies from 0.6Hz to 9Hz. These variations in the low cutoff frequency can be significantly reduced by varying the integrator capacitance C_{int} along with the adjustment of gain. As shown in Fig. 18 variations in the low cutoff frequency are maintained within a range of 8.97Hz to 9.86Hz. Fig. 19 shows the AC response of the conventional inverting amplifier, it can be seen that this scheme suffers from large bandwidth variations that range from 42.79MHz to 1.95MHz within the gain range of 1 to 32.

TABLE 4. Comparison with other related works.

Parameters	[19] 2014	[20] 2015	[21] 2017	[22] 2017	[4] 2018	This work
CMOS technology (μm)	0.35	0.13	0.18	0.18	0.18	0.18
Topology[a]	FD	FD	FD	FD	SE	FD
Configuration[b]	GD	GD	BD	GD	GD	GD
Results[c]	Exp	Exp	Sim	Exp	Exp	Sim
Supply voltage (V)	2.5	1.2	0.3	1.8	$\pm$0.9	$\pm$0.45
Supply current (μA)	0.35	329	0.32	540	100	900
Power dissipation (μW)	0.87	395	0.096	972	180[d]	810
C_L (pF)	—	1	5	2	22	15
SR (V/μs)	—	—	0.0021	—	—	0.51
Gain range (dBs)	10-40	0-20	0-18	0-14	0-23.52	0-30
BW constant with gain	No	Yes	No	Low variations	Yes	Low variations
f_L (Hz)	0.5	NA	NA	NA	2	8.97-9.86
f_H (MHz)	0.001	2.8[e]	0.00295 [f]	30	2.6	9.08-9.54
FOM_{SS} (MHz pF/mW)	—	70	15.4[g]	309	4760[h]	5380
FOM_{LS} ((V/ns)*pF/mA)	—	—	0.0326	—	—	0.0085
Input noise V_{rms} (μV)	2.8	—	—	—	18	—
Input noise ($nV/\sqrt{Hz}$)	—	62	1780	56	—	341
THD (%)	< 1	< 1	1	$0.3 < 1$	0.047	

NOTES:
[a] FD: fully differential, SE: Single-ended.
[b] GD: gate-driven, BD: Bulk-driven.
[c] Exp: experimental, Sim: simulation, PLSim: post-layout simulation.
[d] Without including power dissipation ($P_{dissCnt} = 0.075\mu W$) of a control circuit.
[e] Constant for all gains.
[f] At minimum gain.
[g] Considering BW at maximum gain.
[h] Single-ended schemes double their large and small FOM.

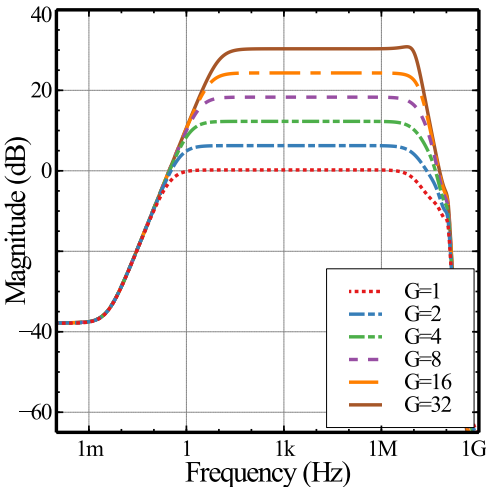

FIGURE 17. Frequency response of LOTA-TRA amplifier with SL.

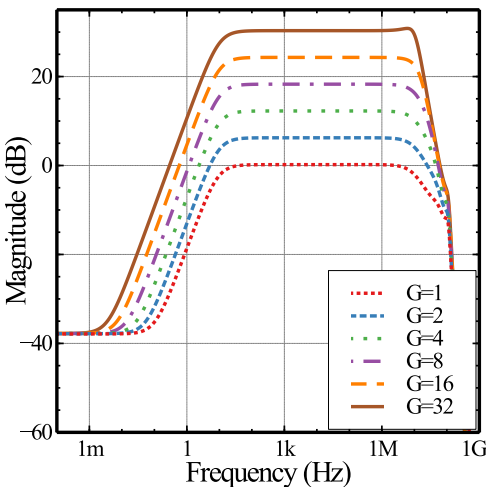

FIGURE 18. Frequency response of LOTA-TRA amplifier with SL and constant 5Hz low cutoff frequency.

The total quiescent power dissipation is 0.81mW for the LOTA-TRA and 630μW for the conventional fully-differential inverting amplifier. The performance of the proposed circuit and the conventional amplifier can be compared using the small signal and large signal figures of merit given by $FOM_{SS} = (GBW \cdot C_L)/P_{Diss}$ and $FOM_{LS} = (SR \cdot C_L)/I_{Qtotal}$ respectively, where I_{Qtotal} is the total quiescent current. Having both the same load capacitance $C_L = 15pF$, the LOTA-TRA prevails upon the conventional as the gain increases. At the maximum gain the LOTA-TRA exhibits a $FOM_{SS} = 5380(MHz * pF/mW)$ while the conventional inverting amplifier has a $FOM_{SS} = 1000(MHz * pF/mW)$. The conventional inverting amplifier and the proposed VGA use the same output stage and they exhibit the same slew rate performance $SR = 0.505$V/us. This SR leads to a large signal figure of merit $FOM_{LS} = 0.0085(V/ns) \cdot pF/(mA)$ in the proposed architecture. On the other hand, the conventional inverting amplifier has a slightly higher large signal figure of merit $FOM_{LS} = 0.0121(V/ns) \cdot pF/(mA)$ but at the expense of loading the signal source and not cancelling the offset and/or input common mode signals. Despite wide gain variation, the bandwidth of the proposed scheme has moderate changes compared to the large bandwidth changes in the conventional amplifier. In Table 4 a comparison with other works is summarized. It must be pointed out that the

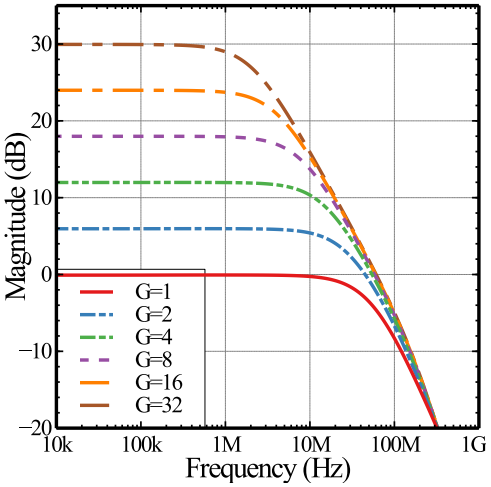

FIGURE 19. Frequency response of the conventional inverting amplifier of Fig. 1.

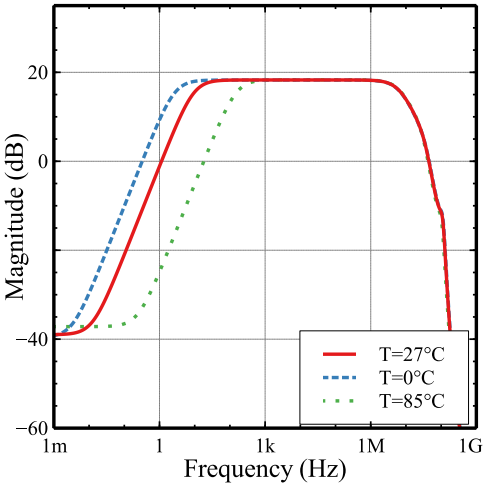

FIGURE 21. Temperature corner simulation of the proposed VGA configured for a gain of 8.

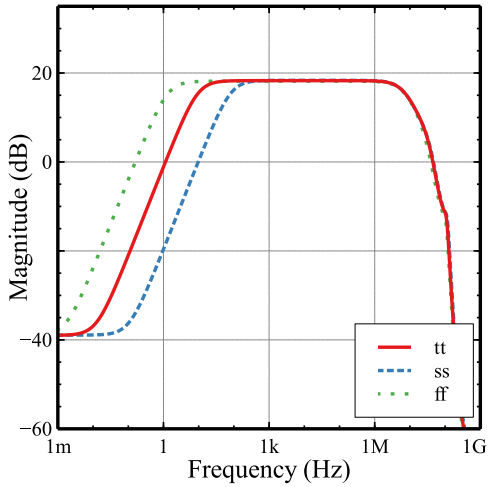

FIGURE 20. Process corner simulation of the proposed VGA configured for a gain of 8.

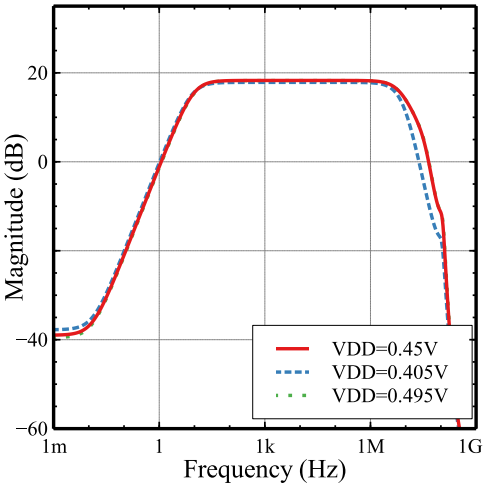

FIGURE 22. Supply voltage corner simulation of the proposed VGA configured for a gain of 8.

proposed circuit has performance characteristics that no other circuit reported in literature has: low supply voltage, wide linear input range, constant bandwidth, high input impedance and DC and offset rejection. A fair comparison would require to compare against other VGA circuits that have all these characteristics together.

The circuit was also simulated for much low power operation using $I_{bias} = 0.5\mu$A and $V_{DD} = -V_{SS} = 0.35$V leading a total power dissipation $P_{Diss} = 10.7\mu$W. The same load capacitance and gain adjustment range were used: $C_L = 15$pF and $G = 1-32$. The bandwidth was reduced to approximately 64kHz with 2% variations over the gain adjustment range. It can be seen that it leads to a power dissipation reduction by approximately two orders of magnitude and, as expected, to a bandwidth reduction by approximately the same factor. By further reduction of the bias current the power dissipation can be reduced by even a larger factor.

PVT corners simulations were performed to evaluate the robustness of the proposal against PVT variations. Fig. 20 shows the simulation for the process corners tt, ss and ff. The simulation for temperature values 0°C, 27°C and 85 °C is depicted in Fig. 21. Supply voltage $V_{DD} = 0.405$V, 0.450V and 0.495V equivalent to 10% were simulated and are shown in Fig. 22. The results show that the design has very small BW variations under the process, voltage or temperature corners. Process and temperature only affect the low cutoff frequency while voltage affects the high cutoff frequency by approximately 10% when the voltage drops by the same percentage.

IV. CONCLUSION

A low-voltage linear VGA with high input impedance capable to operate with $\pm 0.45V$ and wide linear input/output range, designed in 180nm CMOS technology was introduced. The bandwidth changes of 5% from 9.08MHz to 9.54MHz over a gain range from 1 to 32 whereas in the conventional amplifier it changes from 42.79MHz to 1.95MHz.

The proposed scheme exhibits a DC attenuation of 38dB and a low cutoff frequency of 9.86Hz with a power dissipation of 0.81mW.

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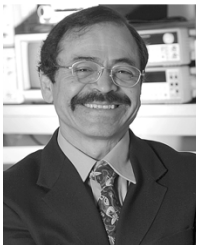

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